**Designing a Single-Ended Differential Pair with Active Loads and Current Mirrors**

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Table of Contents

Introduction………………………………………………………………………...1  
Discussion………………………………………………………………………….1  
Testing and Simulation Analysis…………………………………………………..3  
Conclusion………………………………………………………………………....7  
Appendix…………………………………………………………………….……..9

**INTRODUCTION**

## The aim of this project is to design an operational amplifier using the given design specifications and restraints, and test the amplifier in several different cases. A differential amplifier design was chosen to most effectively achieve design constraints, and active loads and current mirrors were used to minimize signal distortion while maximizing gain. Cadence was used to design, simulate, and implement the amplifier.

## This report aims to detail several decisions and analyses made during the design of the amplifier to minimize power consumption and maximize the swing of the output voltage.

## DISCUSSION

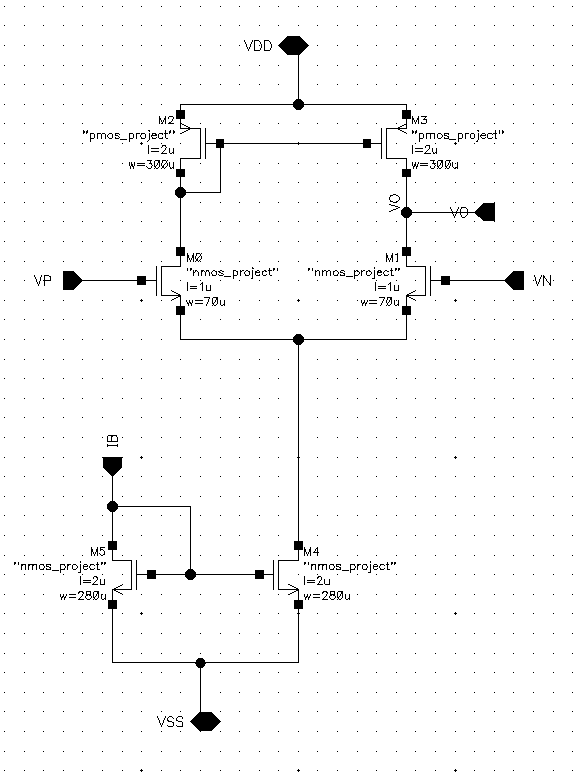
*DESIGN SPECIFICATION*

The following design specifications and constraints were followed when designing the differential amplifier:

1. Overdrive Voltage is greater than or equal to 100mV
2. For open loop testing:
   1. A gain of 100 V/V
   2. A peak to peak output swing of 1V
3. For closed loop testing
   1. A gain of -4 V/V
   2. A peak to peak output swing of 1V when applying a 250mV AC signal

The following default values were used for the transistors:

*HARDWARE DESIGN*

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*Figure 1: Differential Amplifier Design with Active Loads and Current Mirrors*

The design in Figure 1 was used to create the differential amplifier. At the top of the circuit is a PMOS current mirror containing transistors M2 and M3 that are also acting as active loads for the NMOS differential pair transistors of M0 and M1 below them. Below the differential pair is an NMOS current mirror with M4 and M5, and are connected to the DC current source and the drain current of the differential pairs through their drain terminals.

Since the PMOS current mirror also act as active loads for the differential pair, the impedance of the PMOS current mirror is essentially the intrinsic channel length resistance of M2 and M3. In addition, the DC current source with the NMOS current mirror is shorted in small-signal analysis, and therefore the source terminals of the differential pairs can be considered as connected to ground.

After these simplifications, the overall circuit is reduced to two simple common-source amplifier circuits with resistors at their drain terminals. With the simplified circuit containing the same values for each half of the circuit, half circuit analysis can be done instead.

The assumption is made throughout that all the transistors are operating in the saturation region, and therefore the saturation transconductance equation and the intrinsic resistance equation were used to simplify the overall system.

&

Since the PMOS mirrors are active loads, the overall gain using half-circuit analysis for open loop is:

The DC drain current is gone from the gain equation, leaving only VDSAT as the only design variable. The gain of the left side of the equation can be substituted by the design value of 100 V/V, and λ is defined as 0.1 from the design specification. With this, arbitrary design values can be chosen for VDSAT, the common-mode voltage, and the DC current source to begin simulations. Further tuning of these design variables can be made to meet the design specification.

## TESTING AND SIMULATION ANALYSIS

## Multiple simulations were ran to meet the design specifications in open loop and close loop configurations. A common-mode voltage source of 750mV and a 100µA current were used for all the simulations. The following sections breaks down the results of the simulations for both open loop and close loop.

## *OPEN LOOP TESTS*

## 

## *Figure 2: DC operating points and voltages for Open Loop*

## The DC operating points of the open loop test is shown in the figure above. The VDSAT of all the transistors were all slightly above the minimum limit of 100mV to minimize power consumption and output voltage clipping. Furthermore, minimizing VDSAT allows for the transistors to have enough headroom to operate in the saturation region and decreases.

## For open loop testing purposes, a very small DC offset voltage was applied to the input gates of the differential pairs to equalize the drain current flowing through both sides of the circuit. Without this DC voltage offset, the imbalance in drain currents affects the operating region of the transistors, causing the voltage swing to clip when an AC signal is applied. With the DC offset voltage being applied, the output voltage swing can be seen in Figure 3:

## 

## *Figure 3: Open Loop Output Voltage Swing*

## The graph shows that the output swing is around 1V without any clipping at the top or bottom of the sine wave. This test was done using the following equation to find the correct AC input signal that can be applied without clipping the voltage swing:

## The design specifies that and was chosen to simplify calculations. Using the equation above, it can be seen that .

## With the output swing validated to be, an AC analysis was done to find the experimental gain, which can be seen below in Figure 3. From the graph, the gain is around 101 V/V which is within the margin of error to the theoretical gain of 100 V/V

## 

## *Figure 4: Open Loop Gain*

## *CLOSED LOOP TESTS*

## After verifying the open loop results and simulations, the circuit below was then used to simulate a closed loop test.

## 

## *Figure 5: Closed Loop Testing Configuration*

## The configuration uses a negative feedback loop with resistor values of and to achieve a gain close to of -4 V/V. The following figure shows an AC analysis that was done to find the closed loop gain of the circuit:

## 

## *Figure 6: Closed Loop Gain*

## The magnitude of the gain for the simulation came out to be 3.8 V/V which is within the margin of error for a theoretical value of 4 V/V. Looking inside amplifier shows that the designed circuit operates within the limits of the design specification for the VDSAT.

## 

## *Figure 7: DC Operating Points for Closed Loop*

## After confirming that the transistors are still operating within the saturation region based upon the VDSAT values within Figure 6, the output voltage swing can be seen to be around 1V below. A 250mV AC signal was applied as input to find the voltage swing.

## 

## *Figure 8: Closed Loop Output Voltage Swing*

**CONCLUSION**

*SIMULATION ANALYSIS*

As previously stated, the project was successfully developed and implemented. Since the amplifier that was designed is not ideal, the results from the simulation are slightly off from the expected values. The amplifier has intrinsic impedances throughout the circuit that stops the closed loop gain magnitude from being 4 V/V. However, large resistors values can be used in closed loop analysis to boost the closed loop gain very slightly. From Figure 5, applying node voltage analysis at the node VN explains the difference between the theoretical and experimental magnitude of the gain.

Applying equations (1) and (2) to each other and where for the open loop gain:

Calculations for closed loop gain completely matches with the value given by the simulations. On another note, the VDSAT’s of the PMOS current mirror transistor M3 and the NMOS differential pair transistor M1 were different than the open loop simulations. This change in VDSAT values can attribute to the non-ideality factor within the amplifier, and can be part of the explanation on why the simulated closed loop gain is lower than the expected closed loop gain.

*POWER DISSIPATION*

Power dissipation was calculated using the closed loop configuration. From Figure 5, the current flowing through the small-signal input source is 2.331nA based on DC simulations. Using the common-mode voltage and the given current, power can be calculated as:

*SUMMARY OF DESIGN AND PROBLEMS*

The aim of the project is to implement and design an operational amplifier. A differential amplifier design was chosen using current mirrors and active loads. Simulations for open loop for the circuit show the that open loop gain is around 101.5 V/V and the output voltage swing is around 1V. Closed loop simulations show a gain of 3.8 V/V and a similar output voltage swing of around 1V. The result from the simulations match closely to the design specification, and several figures of the circuit show that the DC operating points of the circuit indicate that all the transistors are in saturation region with VDSAT to be over 100mVand VDS to be much larger than VDSAT.

The main problem, when designing the amplifier, is with the voltage swing clipping at either at the top or bottom. The main contributor to the clipping during open loop simulations was the different drain currents flowing through the two branches in the circuits. Applying a differential DC bias voltage between the two gate inputs equalizes the difference in drain currents, and managed to solve most of the clipping issues for the voltage swing. Fine tuning of the width and length ratios of the both current mirrors managed to decrease VDSAT to just over 100mV, solving the clipping issue.

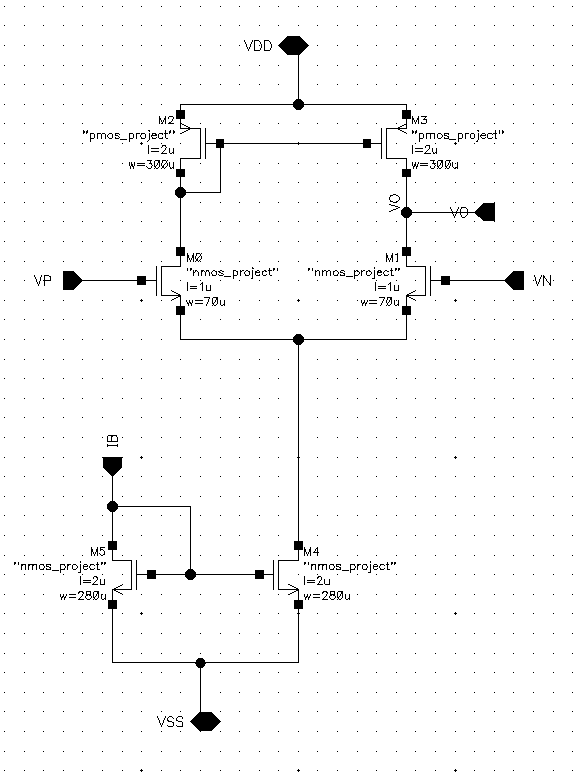
Overall, the designing and implementation of the amplifier is a success as the simulation results match closely to the design constraints. Attached in the appendix is a table of important model parameters for all of the transistors, and larger versions of the figures provided.

**APPENDIX**

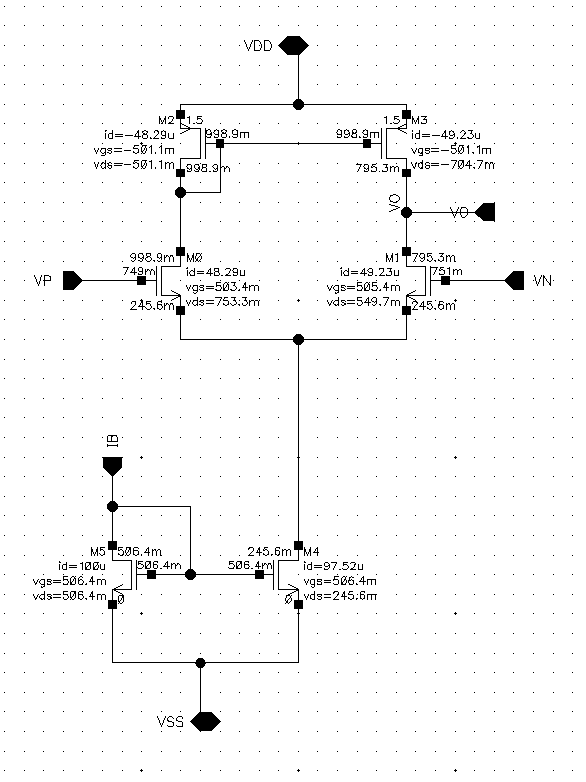
*Appendix A: Table of Model Parameters*

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | M0 | M1 | M2 | M3 | M4 | M5 |
| Gm (µS) | 933.3 | 933.3 | 954.7 | 976.3 | 976.3 | 1.879 |
| Id (µA) | 48.22 | 49.31 | -48.22 | -49.31 | -49.31 | 100 |
| Ro (kΩ) | 15.6 | 10.4 | 10.39 | 14.97 | 14.97 | 5.046 |
| Vbs (mV) | -246.7 | -246.7 | 0 | 0 | 0 | 0 |
| Vds (mV) | 752.3 | 515 | -501 | -738.3 | 738.3 | 506.4 |
| Vdsat (mV) | 103.3 | 105.7 | -101 | -101 | -101 | 106.4 |
| Vgs (mV) | 503.3 | 505.7 | -501 | -501 | -501 | 506.4 |

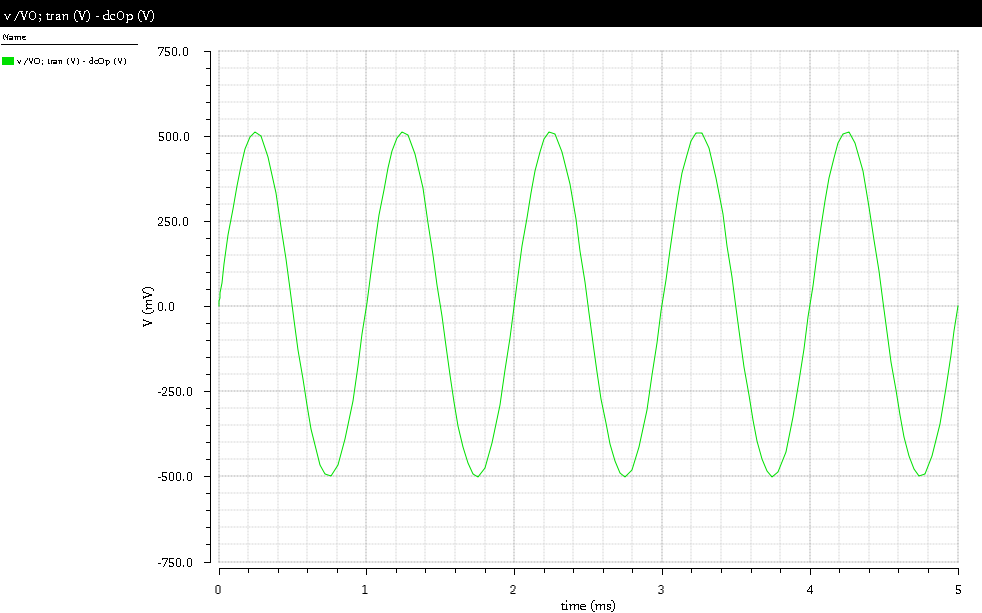
*Appendix B: Figure 1 large version*

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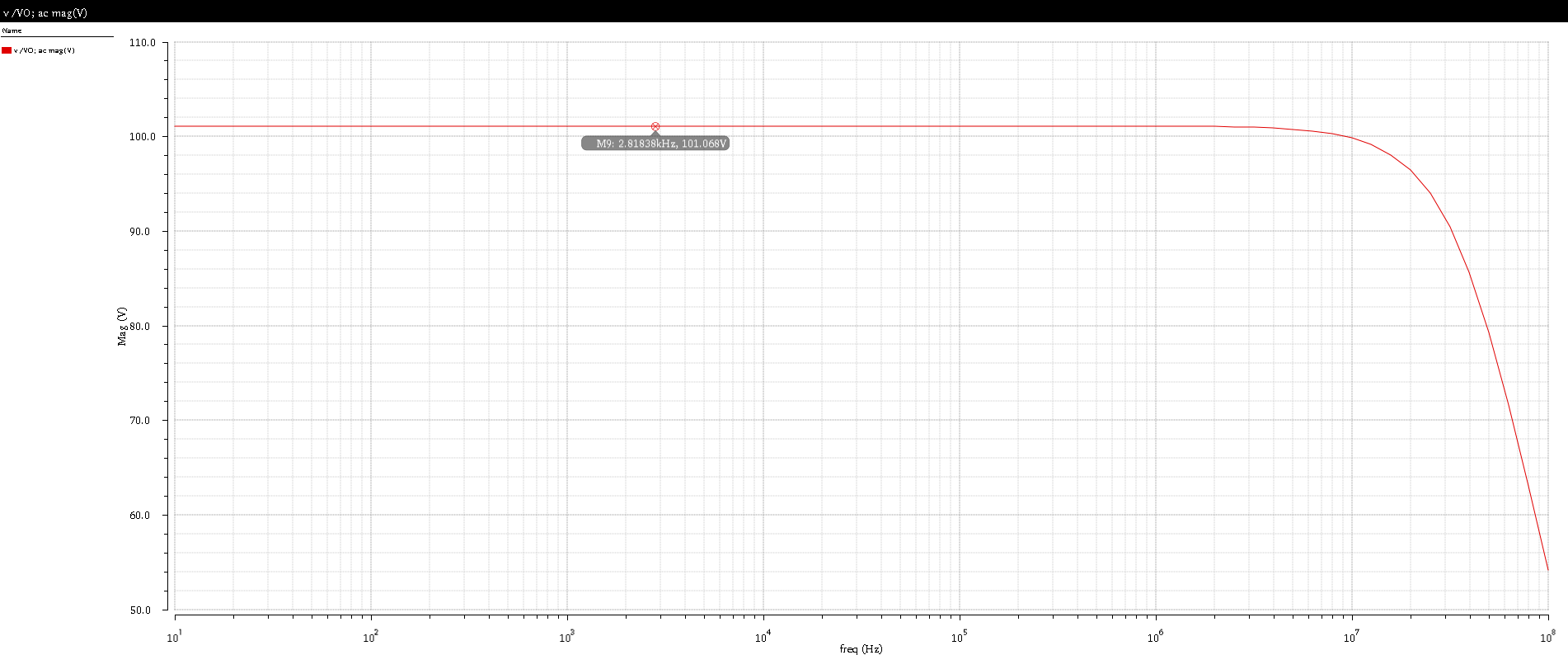
*Appendix C: Figure 2 large version*

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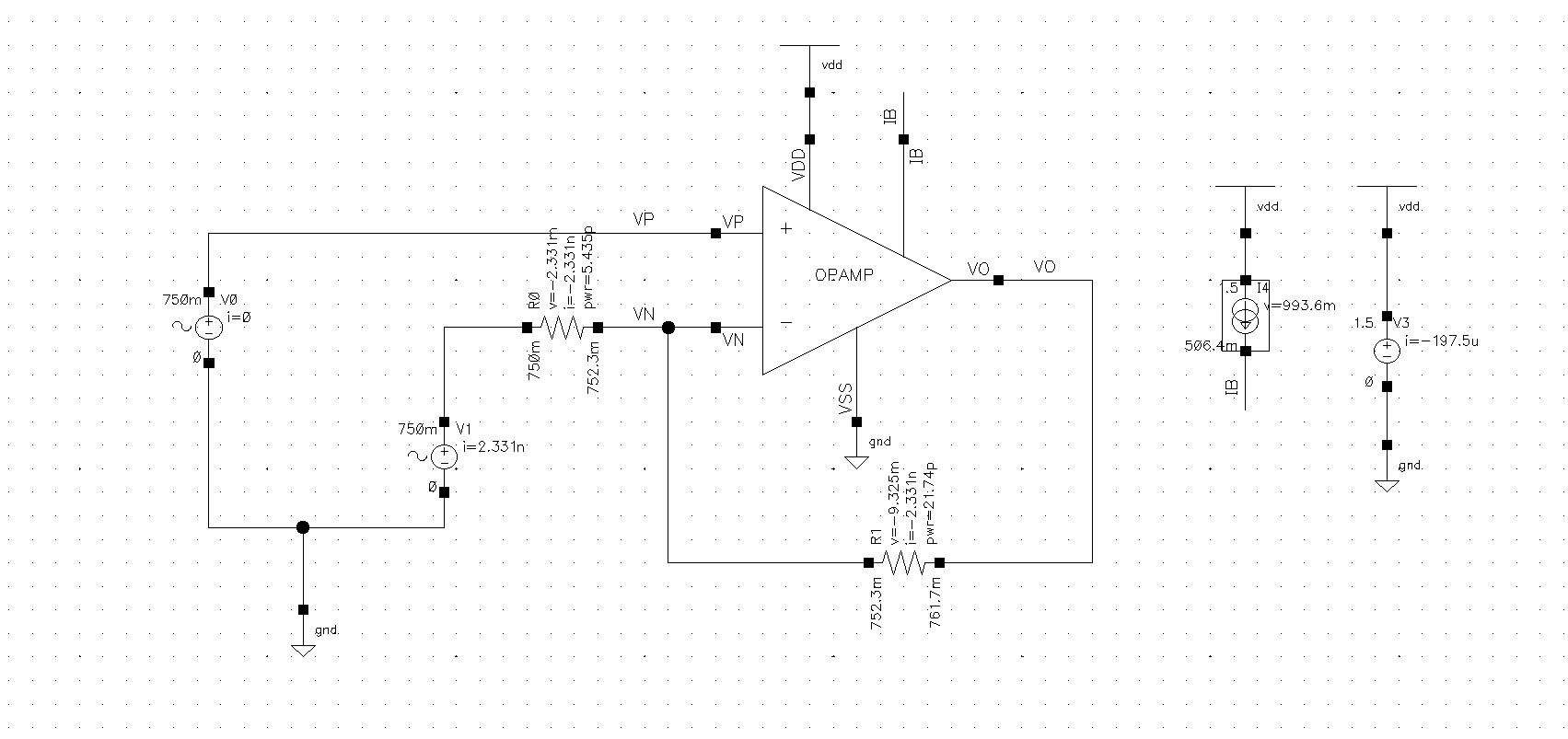
*Appendix D: Figure 3 large version*

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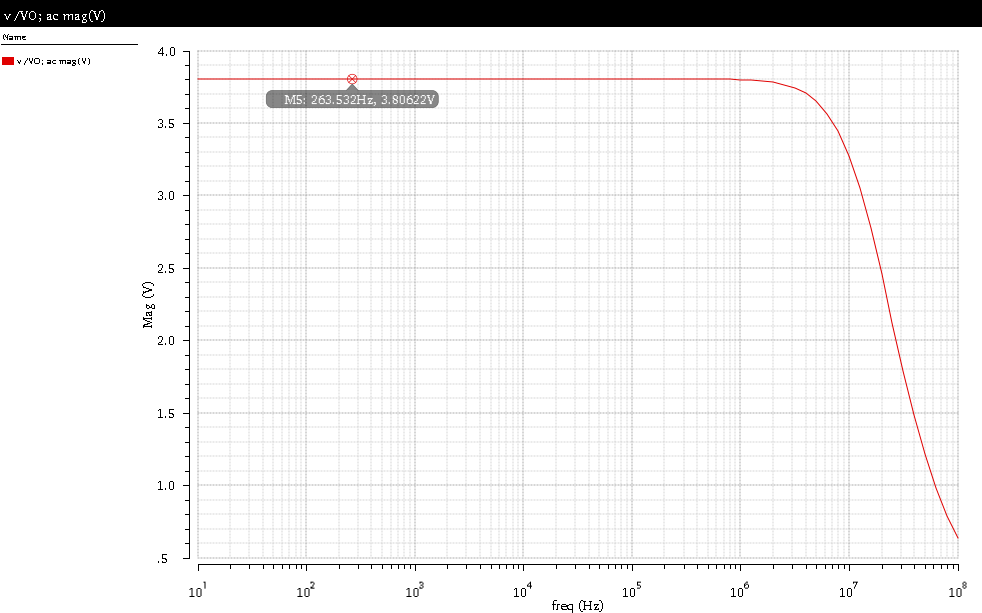
*Appendix E: Figure 4 large version*

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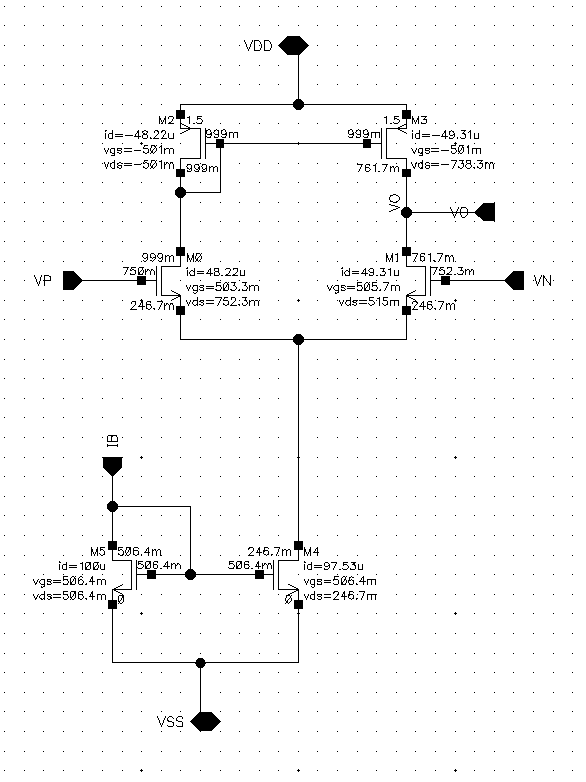
*Appendix F: Figure 5 large version*

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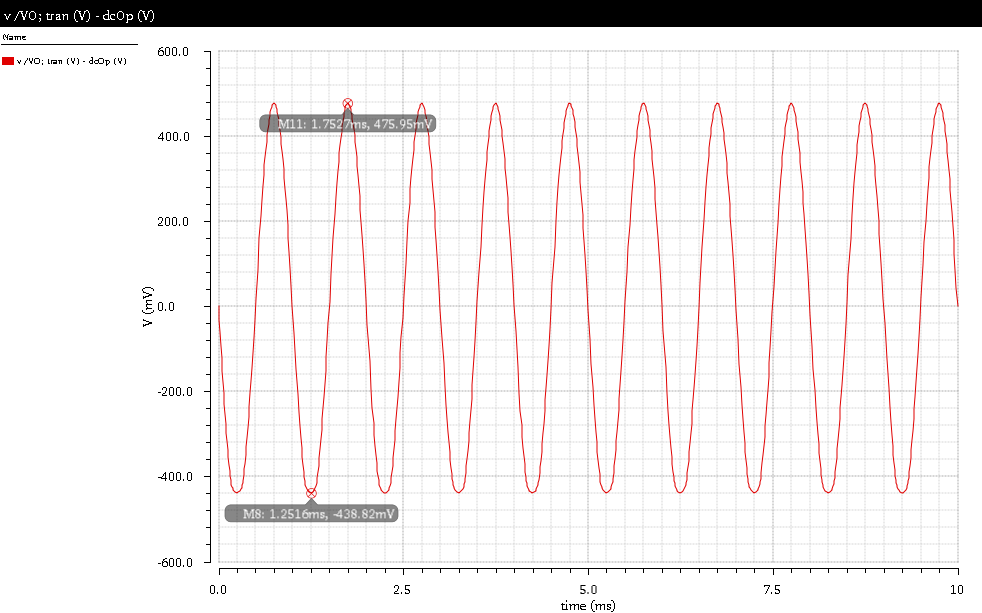
*Appendix G: Figure 6 large version*

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*Appendix H: Figure 7 large version*

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*Appendix I: Figure 8 large version*

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